UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,628	08/19/2003	Robert A. Dunstan	110349-133954	7514

25943   7590   03/17/2009
SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER
BONZO, BRYCE P

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
03/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/644,628	DUNSTAN, ROBERT A.
Office Action Summary	Examiner	Art Unit	
	Bryce P. Bonzo	2113	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>09 February 2009</u>.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-30</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>1-30</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
       1.☐ Certified copies of the priority documents have been received.
       2.☐ Certified copies of the priority documents have been received in Application No. _____.
       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-30 are rejected under 35 USC §103.

Claims 1-30 are rejected under 35 USC §112, first paragraph.

Rejections under 35 USC §112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. Applicant has introduced the term "physically"

into the claims. No support can be found for this terminology. All descriptions of the

negating functions, must be viewed in light of the original disclosure as required in the

Affirmed Appeal. Further, the circuitry switch Applicant is using the basis for their

argument is in fact an advanced controller (item 108, is a bridge controller, a specialized

processor), not a simple transistor as Applicant claims.

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Westerinen (United States Patent Publication No. 2004/0088589) in view of Cooper

(United States Patent No. 5,838,982).

Westerinen discloses:

1. In an apparatus, a method of operation comprising:

receiving a state signal signaling whether the apparatus is in an AC failure state

(¶27 shows the use of switch over signals in a switch over circuit; ¶28 shows the use of

initiate a failover);

receiving a power button event signal signaling an event associated with a power

button of the apparatus (¶21: power button event signal generated and received); and

providing special handling if the state signal signals the apparatus is in the AC

failure state (¶30 describes a specialized handling if power switching is requested

during a power event).

Westerinen does not explicitly disclose:

physically negating the power button event signal if the state signal signals that the apparatus is in the AC failure state.

Cooper discloses these features at Figure 2 the decision tree path corresponding to Blocks 106→108→110→112→END. Column 3, lines 37 disclose the initiation of the this decision tree path. Column 4, lines 9-34 describe this as active code processing in a computer system, and therefore an active decision making process.

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 2-5, Westerinen discloses:

2. The method of claim 1, wherein the method further comprises

monitoring for absence of AC to a power supply of the apparatus (¶26: a switchover circuit monitor for power failure); and

generating a power signal signaling AC failure on detection of absence of AC to the power supply. (¶27: signal generated by the switch over circuit)

3. The method of claim 2, wherein the monitoring and generating are performed by the power supply (Figure 3, item 76 switchover circuit within power supply).

4. The method of claim 2, wherein the method further comprises a selected one of outputting the power signal as the state signal, and forming the state signal based at least in part on the power signal (¶33: outputting signal indicates the power state of the system).

5. The method of claim 1, wherein the event associated with a power button of the apparatus comprises a power button being pressed event (¶21: event signal is generated when the button is pressed).

As per claim 6, Cooper discloses:

6. The method of claim 1, wherein the physically negating comprises combining the state signal and the power button event signal (Figure 2,item 112 and column 3, lines 33-65 the power event button is ignored if the system does not have available power)

As per claim 7, Westerinen discloses:

7. The method of claim 1, wherein the method further comprises

receiving a device wake event signal signaling a device wake event of the

apparatus (¶21: event signal generated when button is depressed);

As per claim 7, Cooper discloses:

physically negating the device wake event signal, if the state signal signals that

the apparatus is in the AC failure state (Figure 2,item 112 and column 3, lines 33-65 the

power event button is ignored if the system does not have available power).

Cooper discloses:

negating the device wake event signal, if the state signal signals the apparatus is in the

AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event

signal ignore if system does not have available power source (AC failure state)].

As per claim 8, Westerinen discloses:

In an apparatus, a method of operation comprising:

receiving a state signal signaling whether the apparatus is in an AC failure state

[para 0027: signals generated by, switchover circuit];

receiving a device wake event signal signaling a device wake event of the

apparatus [para 0021 : power button event signal generated and received]; and

negating the device wake event signal if the state signal signals the apparatus is in the

AC failure state.

Westerinen does not disclose:

physically negating the device wake event signal if the state signal signals that the
apparatus is in the AC failure state.

Cooper discloses:

negating the device wake event signal if the state signal signals the apparatus is in the
AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event
signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose
negating the power button signal if the system is in an AC failure state, however Cooper
does. Cooper discloses a system that determines if the system has available power
before powering up and if there is no power, the system ignores (negates) the power on
signal. Negating the power on signal while in a power failure state is well known in the
art and power efficient. Westerinen does explicitly disclose concern about draining the
battery power (power efficiency) [para 0030: mechanism to only power up the system
when there is a steady power supply]. Thus it would have been obvious to one of
ordinary skill in the art at the time of invention to negate the power button event signal
when the system is in a power failure state as taught in Cooper into the system of
Westerinen to create a more power efficient system.

9. The method of claim 8, wherein the method further comprises

monitoring for absence of AC to a power supply of the apparatus (¶26:

switchover circuit monitor for power failure); and

generating a power signal signaling AC failure on detection of absence of AC to the

power supply (¶27: signals generated by switchover circuit).

10. The method of claim 9, wherein the monitoring and generating are performed by the

power supply (Figure 3, reference 76: switchover circuit within power supply).

11. The method of claim 9, wherein the method further comprises a selected one of

outputting the power signal as the state signal, and forming the state signal based at

least in part on the power signal (¶33: outputting signal indicate the power state).

As per claim 12, Westerinen discloses:

The method of claim 8, wherein the physically negating comprises combining the state

signal [para 0033: power state signal] and the device wake event signal [para 0021:

power button signal].

Westerinen does not disclose:

The method of claim 8, wherein the negating comprises combining the state signal and

the device wake event signal.

Cooper discloses:

wherein the physically negating comprises combining [Figure 2, reference 112 and column 3, lines 33-65: power button event signal is ignore (negating) if system does not have available power source (AC failure state)] the state signal and the power button event signal.

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 13, Westerien discloses:

13. A system comprising:

an arrangement to generated a state signal signaling whether the system is in an AC

failure state [para 0027 and Figure3: arrangement to generate a state signal]; and

a first circuit coupled [Figure 3, reference 36: controller] to the arrangement to receive

the state signal and a power button event signal indicating an event associated with a

power button of the system [para 0021 and para 0033: power button event signal and

state signal received by controller], and

Westerinen does not disclose:

to physically negate the power button event signal if the state signal signals the AC

failure state.

Cooper discloses:

to negate the power button event signal if the state signal signals the AC failure state

[Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if

system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose

negating the power button signal if the system is in an AC failure state, however Cooper

does. Cooper discloses a system that determines if the system has available power

before powering up and if there is no power, the system ignores (negates) the power on

signal. Negating the power on signal while in a power failure state is well known in the

art and power efficient. Westerinen does explicitly disclose concern about draining the

battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

14. The system of claim 13, wherein the system further comprises a monitor to monitor for presence or absence of AC to a power supply of the system (¶26: switchover circuit monitor for power failure), and to generate a power signal signaling accordingly. (¶27: signals generated by switchover circuit)

15. The system of claim 14, wherein the system further comprises the power supply, and the monitor is an integral part of the power supply (Figure 3, reference 76: switchover within power supply).

16. The system of claim 14, wherein the system further comprises a second circuit (Figure 3: switch over circuit) coupled to the power supply and the first circuit, to generate the state signal based at least in part on the power signal, and to provide the first circuit with the state signal (29: generate signal to indicate state).

17. The system of claim 13, wherein the first circuit comprises a signal combiner circuit element to combine the state signal and the power button event signal (figure

3,reference 36, 86 and 50: state and power button event signal combined in controller, signal circuit is therefore inherent).

As per claim 18, Westerinen discloses:

 The system of claim 13, wherein the system further comprises at least one hardware element equipped to generate a device wake event signal signaling a device wake event of the system (¶29); and

Westerinen does not disclose:

the first circuit is also equipped to physically negate the device wake event signal, if the state signal signals the apparatus is in the A C failure state.

Cooper discloses:

the first circuit is also equipped to negate the device wake event signal, if the state signal signals the apparatus is in the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

19. The system of claim 13, wherein the system further comprise a networking interface(¶21: LAN and modem communication can trigger a wake up event (networking interface is inherent).)

As per claim 20, Westerinen discloses:

A system comprising:

    an arrangement to generate a state signal signaling whether the system is in an AC failure state [para 0027 and Figure3: arrangement to generate a state signal]; and

    a first circuit coupled [Figure 3, reference 36: controller] to the arrangement to receive the state signal and a device wake event signal signaling a device wake event of the system [para 0021 and para 0033: power button event signal and state signal received by controller], and

    to negate the device wake event signal if the state signal signals that the AC failure state.

    Westerinen does not disclose:

    to physically negate the power button event signal if the state signal signals the AC failure state.

    Cooper discloses:

to physically negate the power button event signal if the state signal signals the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose

negating the power button signal if the system is in an AC failure state, however Cooper

does. Cooper discloses a system that determines if the system has available power

before powering up and if there is no power, the system ignores (negates) the power on

signal. Negating the power on signal while in a power failure state is well known in the

art and power efficient. Westerinen does explicitly disclose concern about draining the

battery power (power efficiency) [para 0030: mechanism to only power up the system

when there is a steady power supply]. Thus it would have been obvious to one of

ordinary skill in the art at the time of invention to negate the power button event signal

when the system is in a power failure state as taught in Cooper into the system of

Westerinen to create a more power efficient system.

21. The system of claim 20, wherein the system further comprises a monitor to monitor

for presence or absence of AC to a power supply of the system (¶26), and to generate a

power signal signaling accordingly (¶27)

22. The system of claim 21, wherein the system further comprises the power supply,

and the monitor is an integral part of the power supply (Figure 3, reference 76:

switchover circuit within power supply).

23. The system of claim 21, wherein the system further comprises a second circuit

(Figure 3, reference 86: switch over circuit) coupled to the power supply and the first

circuit, to generate the state signal based at least in part on the power signal, and to

provide the first circuit with the state signal (¶29: generate signal to indicate state).

24. The system of claim 20, wherein the first circuit comprises a signal combiner circuit

element to combine the state signal and the device wake event signal (Figure 3, items

36, 86 and 50)

25. The system of claim 20, wherein the system further comprise a networking interface

(¶21).

As per claim 26, Westerinen discloses:

    An apparatus comprising:

    a first input terminal [Figure 3, reference 86 to 36: input terminals to the

controller] to receive a first signal indicating presence or absence of AC to a power

supply of a system [para 0027: signals generated by switchover circuit to the controller];

    a second input terminal to receive a second signal indicating a power button

event of the system apparatus [Figure 3, reference 50: power button event signal across

a second input terminal on a controller]; and

    a first combiner circuit element coupled to the first and second input terminals to

combine the two signals [Figure 3, references 36, 38, and 50: state signal and power

button event signal combined in controller, signal combiner circuit inherent] to negate

the second signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

to physically negate the second signal whenever the first signal signals absence of AC to the power supply.

Cooper discloses:

to physically negate the second signal whenever the first signal signals absence of AC to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and is power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 27, Westerinen discloses:

The apparatus of claim 26, wherein the apparatus further comprises

a third input terminal to receive a third signal indicating a device wake event of the system [Figure 3, reference 26 and para 0029: battery driver supplies a wake signal to the controller through a third input terminal]; and

a second combiner circuit element coupled to the first and third input terminals to combine the two signals [Figure 3, references 36, 26, and 50: state signal and power button event signal combined in controller, signal combiner circuit inherent] to negate the third signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

physically negate the third signal whenever the first signal signals absence of AC to the power supply.

Cooper discloses:

negate the third signal whenever the first signal signals absence of AC to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)]

As per claim 28, Westerinen discloses:

The apparatus of claim 27, wherein the first and third terminals are one of the same terminal [Figure 3, references 36: controller (a terminal in general) functions as both the first and third terminals (one of the same)] and the first and second signal combiner circuit elements are one of the same signal combiner circuit element [Figure 3, references 36: controller (combiner circuit) can perform both functions of the first and second circuits (one of the same)].

As per claim 29, Westerinen discloses: An apparatus comprising: a first input terminal [Figure 3, reference 86 to 36: input terminals to the controller] to receive a first signal indicating presence or absence of AC to a power supply of a system [para 0027: signals generated by switchover circuit to the controller];

a second input terminal to receive a second signal indicating a device wake event of the system [Figure 3, reference 50: power button event signal (device wake event) across a second input terminal on a controller]; and

a first combiner circuit element coupled to the first and second input terminals to combine the two signals [Figure 3, references 36, 38, and 50: state signal and power button event signal combined in controller, signal combiner circuit inherent] to negate the second signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

to physically negate the second signal whenever the first signal signals absence
of AC to the power supply.

Cooper discloses:

to physically negate the second signal whenever the first signal signals absence of AC
to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button
event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose
negating the power button signal if the system is in an AC failure state, however Cooper
does. Cooper discloses a system that determines if the system has available power
before powering up and if there is no power, the system ignores (negates) the power on
signal. Negating the power on signal while in a power failure state is well known in the
art and is power efficient. Westerinen does explicitly disclose concern about draining the
battery power (power efficiency) [para 0030: mechanism to only power up the system
when there is a steady power supply]. Thus it would have been obvious to one of
ordinary skill in the art at the time of invention to negate the power button event signal
when the system is in a power failure state as taught in Cooper into the system of
Westerinen to create a more power efficient system.

As per claim 30, Westerinen discloses:

The apparatus of claim 29, wherein the first and second input terminals are input pins

[Figure 3, reference 36: input terminals are pins].

Response to Applicant's Arguments

Applicant has added, without support or any clear definition, the word *physically*

to the claims. While Applicant provides a very lengthy and contrived definition and

rationale on how *physically* over comes the prior,. the claims remain rejected. There is

no support for this amendment, and when reviewed, the specific does not teach any

physical negation as described by Applicant. In fact, Applicant uses a specialty

controller running firmware (the controller 108), which Applicant's amendment and

resulting arguments argue against. Further, the only support for a negating in any

manner comes from a drawn of a logical AND gate. At no point does Applicant describe

how this is implemented in the physical word, within the specification.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-

3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bryce P Bonzo/
Primary Examiner, Art Unit 2113